REMARKS

Reconsideration of this application, as amended, is respectfully requested. Claims 1-29 are pending. Claims 1-29 are rejected.

Claims 1, 14, 22, and 27 have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Rejections Under 35 U.S.C. § 103

Claims 1-9, 14-19, 21-25 and 27 - 29 have been rejected under 35 U.S.C. 103(a) as being unpatentable over "Value Speculation Scheduling for High Performance Processors" by Fu et al. (art of record, "Fu"), in view of U.S. Patent No. 4,763,245 to Emma, et al. ("Emma").

Applicants have amended claim 1 to include predicting the outcome of the first instruction the predicting comprising inserting a third instruction to be executed after the second instruction and before the first instruction, wherein the third instruction is to retrieve a predicted outcome of the first instruction from the software structure using the outcome of the second instruction as the key into the software structure. The software structure includes a set of keys representing various outcomes of the second instruction and a corresponding set of predicted outcomes of the first instruction.

Fu discloses hardware based value predictors (Figures 5 and 6). More specifically, Fu discloses last value predictors, stride predictors, and value history pattern predictors that predict the values of the instructions using past history associated with the execution of these instructions (col. 1, lines 6-27).

Emma discloses using the branch history table (BHT) to predict the outcomes of branches (col. 5, lines 1-11). More specifically, Emma discloses using Data Dependent Branch Table to update the BHT (col. 5, lines 20-26). In particular, Emma discloses that for taken (executed)

branches that were executed by guessing (guessed taken), the target address is tested by comparing the target address of the guessed taken instruction with the target address of the instruction that has been already confirmed (Figure 1, col. 5, line 40-col. 6, line 5). Further, Emma discloses storing the address of this already executed instruction in the DDBT (col. 6, lines 35-60).

It is respectfully submitted that Fu does not teach or suggest a combination with Emma, and Emma does not teach or suggest a combination with Fu. Fu addresses value speculation scheduling. Emma addresses updating of the data history table. It would be impermissible hindsight based on the Applicants' own disclosure, to combine Fu and Emma.

Furthermore, even if Emma and Fu were combined, such a combination would lack predicting of the outcome of the first instruction that involves inserting a third instruction to be executed after the second instruction and before the first instruction, wherein the third instruction is to retrieve a predicted outcome of the first instruction from the software structure using the outcome of the second instruction as the key into the software structure, as recited in amended claim 1.

Therefore, Applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103(a) over Fu in view of Emma.

Given that amended independent claims 14, 21, and 27 contain at least the discussed limitations of amended claim 1, Applicants respectfully submit that claims 14, 21, and 27 are likewise not obvious under 35 U.S.C. § 103(a) over Fu in view of Emma.

Given that claims 2-9, 15-19, 22-25, and 28-29 depend from amended independent claims 1, 14, 21, and 27 respectively, and add additional limitations, Applicants respectfully submit that claims 2-5, 15-18, 22-24, and 28 are likewise not obvious under 35 U.S.C. § 103(a) over Fu in view of Emma.

Claims 10-13, 20 and 26 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Fu, as applied to claims 1, 14 and 21 above, respectively, in view of U.S. Patent No. 6,687,807 to Damron ("Damron").

Damron discloses an additional memory hardware to store prefetch addresses (col. 4, line 37-col. 5, line 27).

It is respectfully submitted that Fu does not teach or suggest a combination with Damron, and Damron does not teach or suggest a combination with Damron. Fu addresses value speculation scheduling. Damron addresses storing prefetch addresses. It would be impermissible hindsight based on the Applicants' own disclosure, to combine Damron and Fu.

Furthermore, even if Damron and Fu were combined, such a combination would lack predicting of the outcome of the first instruction that involves inserting a third instruction to be executed after the second instruction and before the first instruction, wherein the third instruction is to retrieve a predicted outcome of the first instruction from the software structure using the outcome of the second instruction as the key into the software structure, as recited in amended claim 1.

Therefore, Applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103(a) over Fu in view of Damron.

Given that amended independent claims 14, 21, and 27 contain at least the discussed limitations of amended claim 1, Applicants respectfully submit that claims 14, 21, and 27 are not obvious under 35 U.S.C. § 103(a) over Fu in view of Damron.

Given that claims 10-13, 20, and 26 depend from amended independent claims 1, 14, and 22 respectively, and add additional limitations, Applicants respectfully submit that claims 10-13, 20, and 26 are not obvious under 35 U.S.C. § 103(a) over Fu in view of Damron.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Tatiana Rossin at (408) 720-8300.

If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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Date: March 21, 2006 By: _____

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